Department of Technical Education
Board of Technical Examinations, Bengaluru

Course Title	: **Digital Electronics**	Course Code	: **15EC32T**
Semester	: **Third**	Credits	: **4**
Teaching Scheme in Hrs (L:T:P)	: **4:0:0**	Course Group	: **Core**
Type of course	: **Lecture**	Total Contact Hours	: **52**
CIE	: **25 Marks**	SEE	: **100 Marks**

Prerequisites

Knowledge of basics of number systems and digital electronics.

Course Objectives

1. Understand the working of various digital electronics circuits.
2. Apply principles of number systems and Boolean algebra to solve simple logical problems
3. Learn to design the simple digital circuits.
4. Enable to learn principles digital processors in higher learning

Course Outcomes

On successful completion of the course, the students will be able to attain the following COs

	Course Outcome	CL	Linked PO	Teaching Hrs
CO1	Apply the basic knowledge of digital electronics to construct and design simple combinational digital circuits.	*R/U/A*	1,2,3,4,10	**09**
CO2	Construct flip-flop circuits and analyze their functioning	*R/U/A*	1,2,3,4,10	**09**
CO3	Construct counters and shift registers and understand their operation.	*R/U/A*	1,2,3,4,10	**10**
CO4	Understand the functioning of A to D and D to A converters and their relevance.	*R/U/A*	1,2,3,4,10	**09**
CO5	Understand the function and applications of various types of memories and digital IC families.	*R/U/A*	1,2,3,4,10	**09**
CO6	Construct, analyze and verify the functioning of simple digital circuits/ICs using modern tools.	*R/U/A*	1,2,3,4,5,6,7,10	**06**
			Total	**52**

Course-PO attainment matrix

Course	Programme Outcomes									
	1	2	3	4	5	6	7	8	9	10
Digital Electronics	3	3	3	3	1	1	1	--	--	3

Level 3- Highly Addressed, Level 2-Moderately Addressed, Level 1-Low Addressed.

Method is to relate the level of PO with the number of hours devoted to the COs which address the given PO.

If ≥40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 3

If 25 to 40% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 2

If 5 to 25% of classroom sessions addressing a particular PO, it is considered that PO is addressed at Level 1

If < 5% of classroom sessions addressing a particular PO, it is considered that PO is considered not-addressed.

Course content and pattern of marks for SEE

Unit	Unit Name	Teaching Hours	Questions for SEE			Marks	Weightage (%)
			R	U	A		
1	Combinational logic circuits	09	05	10	10	25	17
2	Basic sequential circuits	09	05	05	15	25	17
3	Registers and counters	10	05	10	15	30	20
4	D to A and A to D converters	09	05	10	10	25	17
5	Memories and programmable devices	09	05	10	10	25	17
6	Digital integrated circuits	06	05	05	05	15	12
	Total	**52**	**30**	**50**	**65**	**145**	**100**

Legend: R- Remember, U- Understand, A- Application

Course Contents

Unit 1: Combinational logic circuits   09 Hours

Introduction: Combinational digital circuit. **Multiplexers:** definition, expression, truth-table, realization of simple (2:1) multiplexer using gates, and applications. Application of multiplexers to implement logic gates and simple sum-of-product equations, list of IC multiplexers and their features. Realization of higher-order multiplexer using lower-order multiplexer ICs. **Demultiplexer:** definition, expression, realization of simple (1:2) demultiplexer using gates, truth-table and applications, and list of IC demultiplexers and their features. **Decoders and encoders:** Definition and relevance of decoders and encoders. Logic diagram and truth-table of Decimal-to-BCD encoder and BCD-to-Decimal decoder. Identification of different decoder and encoder ICs. Need, logic diagram and truth table of BCD to 7-segment decoder. Concept and application of simple (maximum 4 bit) priority encoder.

Unit 2: Basic sequential circuits   09 Hours

Introduction to sequential circuits: Comparison of combinational and sequential circuits. Definition of clock and triggering, types of triggering and their symbolic representations in logic circuits/diagrams. **Flip-flops:** Operation, gate-level circuit, symbol, truth-table and timing waveforms of clocked RS flip-flop and J-K flip-flop. Relevance of asynchronous inputs to flip-flops. Race-around problem and remedies, MS flip-flop, D and T flip-flop. Identify and list flip-flop ICs. **Timer 555:** Internal diagram of IC 555 and its application as astable and monostable multivibrators. Flip-flop as bistable multivibrator.

Unit 3: Registers and counters   10 Hours

Registers: Classification of registers, realization of simple (3 or 4 bit) SISO, SIPO, PISO and PIPO using flip-flops, concept of universal shift-register. List shift-register ICs. **Ring counter and Johnson's counter**: 3 bit circuit, truth-table and on applications. **Counters**: definition, modulus, classification (definitions of up/down, asynchronous/synchronous, full-mod/partial-mod) and applications. Working and realization (using flip-flops) of asynchronous and synchronous 3-bit or 4-bit counters, and their comparison. Realization of higher-mod counters using lower-mod counters. List counter ICs and study configuring IC 7490 as decade counter.

Unit 4: D to A and A to D Converters   09 Hours

Data/signal conversion: Concept and need. **DAC:** Definition, symbolic representation, types, and applications. Circuit, functioning and output expression for 3 or 4-bit DAC using Resistive divider and binary-ladder network. DAC specifications- resolution, accuracy, settling time, speed, linearity and monotonicity, and simple problems. Identify IC DACs and list their features. **ADC:** Definition, types, applications, specifications-resolution, accuracy, non-linearity, and conversion time. Working of 3-bit or 4-bit flash type, successive approximation and dual-slope ADCs, and simple problems. Identify IC ADCs and list their features.

Unit 5: Memories and programmable devices   09Hours

Introduction: Definition and relevance of memories. **Classification:** Based on fabrication material, data retention, speed, storage capacity, cost and application. Working principle and features of magnetic memory, ROM, PROM, EPROM, E^2PROM, flash memory, static and dynamic RAM cells, DDR memory & its variants and disk memories. Memory accessing process in semiconductor, magnetic and disk memories. Memory word-size and capacity of memories with examples. **Programmable devices:** Difference between fixed logic and programmable logic, PLA and PAL-architecture, and implementation of simple Boolean equations.

Unit 6: Digital integrated circuits   06 Hours

Logic families: Introduction, classification, definitions of fan-in, fan-out, propagation delay, power dissipation and noise margin. Working and circuit of standard TTL NAND gate and CMOS inverter, voltage levels in TTL and CMOS. Comparison of characteristics ECL, TTL, I^2L and CMOS logic families. Interfacing of TTL and CMOS devices. Features of HMOS and CHMOS families. Concept of ESD and remedy.

References

1. *Digital principles and applications.* Donald P Leach, Albert Paul Malvino, Goutam Saha, McGraw Hill Publisher, 8th edition, ISBN 10: 9339203402 ISBN 13: 9789339203405
2. *Digital Systems-principles and applications.* Ronald J. Tocci, Neal S.Widmer, Gregory L.Moss, 10th edition,ISBN : 0131725793
3. *Digital Electronics* –principles and integrated circuits. Anil K. Maini. Wiley publications,first edition . ISBN: 978-0-470-03214-5
4. *Digital Computer Fundamentals,-* Thomas C Bartee ,McGraw-Hill Publisher,6th edition.ISBN 10: 0070038996 / ISBN 13: 9780070038998
5. *Digital fundamentals* –Floyd and Jain, PEARSON EDUCATION publication, 8th Edition , ISBN-13: 978-0132359238 ,ISBN-10: 0132359235
6. www.nptel.ac.in
7. http://freevideolectures.com/Course/3164/Digital-Electronics
8. http://www.freebyte.com/electronics/
9. https://www.**circuitlogix**.com
10. http://www.vlab.co.in
11. www.electronics-tutorials.ws
12. http://www.allaboutcircuits.com
13. http://ocw.mit.edu/

Course Delivery

The course will be delivered through lectures, presentations and support of modern tools. Student activities are off-class

Course Assessment and Evaluation Scheme

Master Scheme

Assessment Method	What		To Whom	Assessment mode /Frequency /timing	Max. Marks	Evidence Collected	Course Outcomes
Direct assessment	CIE	IA	Students	Three tests[+]	20	Blue Books	1 to 6
				Activity*	05	Activity Sheets	1 to 6
	SEE	End exam		End of the course	100	Answer Scripts at BTE	1 to 6
				Total	125		
Indirect assessment	Student feedback on course		Students	Middle of the Course	Nil	Feedback Forms	1 to 3 Delivery of course
	End of course survey			End of the Course	Nil	Question-naires	1 to 6 Effectiveness of delivery instructions & assessment methods

Legends: CIE-Continuous Internal Evaluation, SEE- Semester End-exam Evaluation

[+] Every I.A. test shall be conducted for 20 marks. Average of three tests, by rounding off any fractional part thereof to next higher integer, shall be considered for IA.

*Students should do activity as per the list of suggested activities/ similar activities with prior approval of the teacher. Activity process must initiated well in advance so that it can be completed well before the end of the term.

Questions for CIE and SEE will be designed to evaluate the various CLs as per the weightage shown in the following table.

Sl. No.	Cognitive Levels (CL)	Weightage (%)
1	Remembering	20
2	Understanding	35
3	Applying	45
	Total	**100**

Continuous internal evaluation (CIE) pattern

(i) Student Activity (5 marks)

The following student activities or similar activities can be assigned for assessing CIE/IA marks

Sl. No.	Activity
1	Collect the information about the different types of display devices used in digital circuits and carry out a seminar
2	Collect the specification sheets, availability and cost of any two ADC and DAC ICs
3	Prepare a block diagram approach to construct a digital clock or a frequency counter or a digital voltmeter or any other similar digital electronic circuits and analyze the cost of the application
4	Prepare a note on E-waste and disposal of PCBs and ICs, carry out a seminar
5	Design and simulate the working of any simple logic circuit using a suitable modern software tool

Execution Notes:
1. Maximum of 2 students in each batch for student activity
2. Above activities may be distributed among different batches; activity No. 5 is mandatory and any one activity among 1 to4 or any similar activities per batch may be assigned by the teacher based on interest of the students.
3. Project activities shall be carried out throughout the semester and present the project report at the end of the semester; concerned teacher is expected to observe and record the progress of students' activities
4. Submit qualitative hand-written report not exceeding 6 pages; one report per batch
5. Each of the activity can be carried out off-class well in advance; however, demonstration/presentation should be done during laboratory sessions
6. Assessment shall be based on quality of work as prescribed by the following **rubrics** table

(ii) Model of rubrics for assessing student activity (for every student)

Dimension	Scale					Marks (Example)
	1 **Unsatisfactory**	**2** **Developing**	**3** **Satisfactory**	**4** **Good**	**5** **Exemplary**	
1. Research and gathering information	Does not collect information relate to topic	Collects very limited information, some relate to topic	Collects basic information, most refer to the topic	Collects more information, most refer to the topic	Collects a great deals of information, all refer to the topic	3
2. Full-fills team roles and duties	Does not perform any duties assigned to the team role	Performs very little duties	Performs nearly all duties	Performs almost all duties	Performs all duties of assigned team roles	2
3. Shares work equality	Always relies on others to do the work	Rarely does the assigned work, often needs reminding	Usually does the assigned work, rarely needs reminding	Always does the assigned work, rarely needs reminding.	Always does the assigned work, without needing reminding	5
4. Listen to other team mates	Is always talking, never allows anyone to else to speak	Usually does most of the talking, rarely allows others to speak	Listens, but sometimes talk too much,	Listens and talks a little more than needed.	Listens and talks a fare amount	3
					Total marks	ceil(13/4)= 4

(iii) CIE/IA Tests (20 Marks)

Three tests have to be conducted, during specified schedule, in accordance with the test pattern given below and their average-marks shall be considered for CIE/IA.

(iv) Format of CIE/IA test question paper

CIE Question Paper					
Institution Name and Code					
Course Coordinator/Teacher					
Program Name		***Test No.***		*Units*	
Class/Sem		*Date*		*CL*	
Course Name		*Time*		*COs*	
Course Code		*Max. Marks*		*POs*	
Note to students: Answer all questions					

Question No.	Question	Marks	CL	CO	PO
1					
2					
3					
4					

Legends: PO-Program Outcome, CO-Course outcome, CL-Cognitive Level, R-Remember, U-Understand, A-Apply
Note: Internal choice may be given in each CO at the same cognitive level (CL)

(v) Model question paper for CIE

CIE Question Paper						
Institution Name and Code						
Course Coordinator/ Teacher						
Program Name	Electronics and Communication	*Test No.*	1	*Units*	1 & 2	
Class/Sem	3rd Sem	*Date*	--/--/----	*CL*	R/U/A	
Course Name	Digital Electronics	*Time*	10-11AM	*COs*	1 & 2	
Course Code	15EC32T	*Max. Marks*	20	*POs*	1& 3	

Note to students: Answer all questions

No.	Question	Marks	CL	CO	PO
1	Define a demultiplexer and construct a 1:4 demultiplexer using logic gates	05	R/A	1	1,2
2	Illustrate use of multiplexer to realize $y=\bar{A}\bar{B}\bar{C} +\bar{A}\bar{B}C+ABC$ OR Show how to realize 2-iput NOR gate using a multiplexer IC	05	A	1	1,2
3	Define combinational and sequential circuits and compare them	05	R/U	2	1,2
4	Identify the problems associated with JK flip-flop and modify JK flip-flop or suggest remedy to overcome the problem OR Write the JK flip-flop gate-level diagram and convert it to D flip-flop	05	A/U	2	1,2

Semester End-exam Evaluation (SEE)

(i) End-exam question-paper pattern

Unit	Unit Name	Study Duration (Hrs.)	No. Questions for end-exam	
			PART – A 5 Marks	PART – B 10 Marks
1	Combinational logic circuits	09	01	02
2	Flip-flops and related circuits	09	01	02
3	Registers and counters	10	02	02
4	D to A and A to D converters	09	01	02
5	Memory devices	09	03	01
6	Digital integrated circuits	06	01	01
	Total	**52**	**09 (45 Marks)**	**10 (100 Marks)**

(ii) Model question paper

Course Title   **: DIGITAL ELECTRONICS**

Course Code   **: 15EC32T**   Time   **: 3 Hrs**

Semester   **: Third**   Max. Marks**: 100**

Instructions*: 1. Answer any **SIX** question from **Part A** (5x6=30 Marks)*

*2. Answer any **SEVEN** full questions from **Part B** (7x10=70 Marks)*

Part A

1. Define combinational and sequential digital circuits with examples.

2. Describe the functioning of RS flip-flop with gate-level circuit and truth table.

3. Define shift register and list different types of data movements in it.

4. Sketch the timing diagram for serial shifting of 101 data in 3-bit shift register.

5. Define resolution, accuracy, settling time, monotonicity, and speed as related to DAC.

6. List the features of magnetic memories.

7. Explain the working principle of Dynamic RAM cell.

8. Compare PLA and PAL.

9. Describe briefly the operation of TTL NAND gate with circuit.

Part B

1. (a) Construct 4:1 multiplexer using 2:1 multiplexers.

   (b) Illustrate use of multiplexer in implementation of simple Boolean functions with example.

2. a) Explain the role of BCD to 7–segment decoder in numbers display.

   b) Discuss the role of control signals in demultiplexer circuit.

3. a) Explain the function of D flip-flop and also write truth-table.

   b) Calculate the frequency at Q of JK flip-flop if it is triggered by 1 KHz clock signal under toggle mode, and sketch the input and output signals.

4. Show how to configure 555 timer as monostable multivibrator and astable multivibrator.

5. Construct a mod-7 counter and explain its functioning with the help of truth table and timing waveforms.

6. Show how to configure 7490 IC as decade counter and write its truth table.

7. Explain a binary ladder network of DAC with expression output. List its advantages.

8. (a) Calculate the resolution of a 4-bit DAC in terms of percentage of full-scale voltage

   (b) For a 5-bit resistive divider, determine the following i) the weight assigned to the LSB. ii) The change in the output voltage due to a change in the LSB. iii) The output voltage for a digital input of 10110. Assume 0= 0 V and 1= + 10 V.

9. a) Calculate the number of address lines required to access 512 Kilo bytes of memory and calculate how many bytes of memory can be accessed with 15 address lines assuming byte addressable memory.

   b) Identify the functional pins required for a typical RAM IC.

10. a) Explain the functioning of CMOS inverter.

    b) List the voltage levels of TTL family.

Institutional activities (No marks)

The following are suggested institutional activities, to be carried out at least one during the semester. The course teacher/coordinator is expected to maintain the relevant record (Containing, Activity name, Resource persons and their details, duration, venue, student feedback, etc) pertaining to Institutional activities.

Sl. No.	Activity
1	Organize Seminar, workshop or Lecture from experts on the modern trends/developments in digital electronics.
2	Organize hands-on practice on design and simulation of digital circuits.
3	Motivate students to take case study on different digital electronics-based mini projects to inculcate self and continuous learning.

Model Question Bank

Note: The questions in the question bank are indicative but not exhaustive. Sub-questions on different CLs may be combined to frame 10-marks questions or 10-marks questions given here can be splitted into 5-marks questions if necessary keeping weightage of CLs approximately intact and adhering to SEE end-exam pattern.

Unit-1: Combinational logic circuits

Five-mark Questions

REMEMBER
1. Define combinational and sequential digital circuits with examples.
2. List any five combinational circuits and state their functions.
3. List any five sequential circuits and state their functions.
4. Define i) encoder, ii) decoder, iii) multiplexer, iv) demultiplexer, and v) priority encoder
5. Describe the demultiplexing function with the help of any demux circuit/IC
6. Describe the working of 4:1 multiplexer with the help of suitable diagram

7. Describe the multiplexing process with suitable digital multiplexer circuit.
8. Describe the working of simple priority encoder
9. Name the pin functions in any typical demultiplexer IC
10. List the truth-table entries of BCD to 7-sgement decoder
11. List the similarities and dissimilarities between encoders and multiplexers
12. Name the applications of multiplexer, demultiplexer, encoder, decoder and priority encoder

UNDERSTAND
1. Explain the working of any decoder with logic circuit
2. Explain the working of encoder with logic circuit
3. Explain how to implement the Boolean function y=$A\bar{B}+\bar{A}B$ using a multiplexer IC
4. Compare encoder and decoder
5. Differentiate between multiplexer and demultiplexer
6. Demonstrate how BCD are displayed using combinational circuit
7. Differentiate between encoder and priority encoder

APPLICATION
1. Show how a 4-to-1 multiplexer can be realized using 2-to-1 multiplexers.
2. Show how to implement NAND function using a multiplexer IC
3. Construct 1:2 demultiplexer using gates and demonstrate its function
4. Write the truth table of 3 bit priority encoder
5. Calculate the control lines needed for 4:1 mux and 1:8 demux sketch the their logic diagrams

Ten-mark Questions

UNDERSTAND
1. Classify the combinational circuits and state the function and application of each category.
2. (a) Explain the role of BCD to 7 –segment decoder in numbers display
    (b) Compare combinational and sequential digital circuits with examples
3. (a) Convert multiplexer to logic gate
    (b) Discuss the role of control signals in demultiplexer circuit.

APPLICATION
1. (a) Construct 4:1 multiplexer using 2:1 multiplexers.
   (b) Illustrate use of multiplexer in implementation of simple Boolean functions
2. (a) Demonstrate the use of BCD to 7-segment decoder in numbers display
   (b) Write simple encoder circuit and its truth-table
3. (a) List any five applications of combinational circuits
   (b) List any five pin functions of multiplexer IC
4. (a) Write simple decoder circuit and its truth table
   (b) List the similarities between demultiplexer and demultiplexer

Unit-2: Flip-flops and related circuits

Five-mark Questions

REMEMBER
1. Define flip-flop and list its applications
2. Describe different types of triggering flip-flops
3. Describe the functioning of RS flip-flop with gate-level circuit and truth table
4. List various flip-flops with logic diagrams.

5. Name the pins and their functions in a typical JK flip-flop.
6. Describe the functioning of D flip-flop with truth table
7. Locate the toggle state in the truth table of JK flip-flop and state its meaning and relevance
8. Describe how flip-flop can be used as divide-by-two counter with relevant waveforms
9. List the pin functions of 555 timer and name any two applications

UNDERSTAND
1. Differentiate between combinational and sequential circuits.
2. Explain the truth table of a D flip-flop and sketch the timing waveforms.
3. Distinguish between Preset and Clear inputs and briefly explain their significance
4. Illustrate race-around problem and discuss how it can be eliminated in JK flip-flops
5. Explain different types of triggering of sequential circuits
6. Modify JK flip-flop into D flip-flop
7. Convert JK into T flip-flop
8. List the ICs of RS, JK, JK-MS, D flip-flops and timer

APPLICATION
1. Calculate the frequency at Q of JK flip-flop if it is triggered by 1KHz clock signal under toggle mode, and sketch the input and output signals.
2. Show how 555 timer can be configured to generate 1KHz clock signal
3. Calculate the pulse width of unstable sate of 555-monostable multivibrator for a 4.7KΩ resistor and a 1.5 μF capacitor.
4. Show how to configure JK flip-flop as D flip-flop with truth table
5. Demonstrate how flip-flop can be used as memory cell

Ten-mark Questions
UNDERSTAND
1. (a) Explain the working of D-flip-flop with relevant diagram and waveform
   (b) Demonstrate conversion of JK flip-flop into T flip-flop
2. (a) Compare sequential circuits with combinational circuits
   (b) Compare T flip-flop with D flip-flop
3. (a) Explain the concept of racing condition and suggest methods to overcome this.
   (b) Show how two JK flip-flops can be cascaded to act as divided-by-4 counter.
4. Explain the working of clocked RS flip-flop with the help of gate-level diagram, truth-table and timing and output wave forms.
5. (a) Compare 555 timer as astable multivibrator and monostable multivibrator
6. (b) Demonstrate how flip-flop can be used as single-bit memory cell.
7. Explain the internal diagram of IC555 timer and name its applications

APPLICATION
1. (a) Illustrate how JK flip-flop can be used as 1-bit memory element.
   (b) Write gate-level circuit of clocked RS flip-flop and its truth table
2. (a) Calculate the frequency of the output at Q of a JK flip-flop when it is triggered by 100Hz signal under toggle state and justify your answer
   (b) List the features of 555 timer IC
3. Show how to configure 555 timer as monostable multivibrator and astable multivibrator

Unit 3: Registers and counters

Five-mark Questions

REMEMBER

1. Describe construction and working of 3-bit shift register
2. Define shift register and list different types of data movements in it
3. Describe the concept of universal shift register and list its applications
4. Define counter, modulus, register, up counting and down counting
5. List the pin functions of a typical IC counter
6. Name the applications of sequential circuits
7. Describe the functioning of mod -8 asynchronous counter with diagram

UNDERSTAND
1. Show how shift register can be realized using flip-flops
2. Explain shifting data bit-by-bit in a 3-bit shift register with relevant diagram
3. Sketch the timing diagram for serial shifting of 101 data in 3-bit shift register
4. Explain the working of 3-bit ring counter with truth-table and logic circuit
5. Compare Ring counter with Johnson counter
6. Differentiate between counter and shift register
7. Identify the applications of shift registers and counters
8. Relate number of flip-flops and modulus of a counter

APPLICATION
1. Write the truth table of 3-bit counter
2. Illustrate 3 bits can be stored in a 3-bit shift register
3. Construct 3-bit shift register to that can allow parallel movement of data
4. List pin functions of a typical shift register IC
5. Sketch the timing diagram/waveforms of a mod-6 counter
6. Sketch the timing diagram/waveforms of 3-bit ring counter
7. Compute the overall modulus of cascaded counter containing mod 2, mod5 and mod3, and justify your answer.

Ten-mark Questions

UNDERSTAND
1. (a) Compare Johnson counter and ring counter.
   (b) Distinguish between synchronous counter and asynchronous counters.
2. (a) Compare SISO and PIPO operation of shift register with examples
   (b) Distinguish between SIPO and PISO operation with examples.
3. Explain the functioning of a 3-bit shift register under SIPO and SISO modes.
4. Describe the operation of mod 8 counter with the help of circuit and truth table

APPLICATION
1. Construct a mod-7 counter and explain its functioning with the help of truth table and timing waveforms
2. (a) Show how flip-flops can be used to realise counter
   (b) List different ways of data movement in shift registers
3. Show how to configure 7490 IC as decade counter and write its truth table
4. (a) Writ the truth table and circuit of mod 5 counter
   (b) Sketch the timing waveforms of a mod 5 counter
5. a) List the applications of counters and shift registers
   (b) Construct a 3-bit counter that circulates the data.

Unit-4: Digital to Analog and Analog to Digital converters
Five-mark Questions

REMEMBER
1. Define resolution, accuracy, settling time, monotonicity, and speed as related to DAC
2. Describe the functioning of a 4 bit ladder-type DAC
3. List the pin functions of a typical DAC IC
4. Describe briefly the operation of a 4-bit SAR DAC
5. List the specifications of ADC and define them
6. List the features of flash-type ADC

UNDERSTAND
1. Distinguish between DAC and ADC
2. Explain the need for ADC and DACs in computing
3. Identify the pins of a typical ADC IC and state their functions
4. Identify the different parts of SAR ADC and state their functions
5. Classify DAC circuits and compare them
6. Compare the features of SAR ADC with Dual slope ADC

APPLICATION
1. An 8-bit DAC produces an analog output of 12.5 mV for a digital input 00000010. Determine the analog output for a digital input of 00001011
2. Determine the resolution of a 12-bit A/D convertor having a full-scale analog input voltage of 5V.
3. An 8-bit D/A convertor has a step size of 20mv.Determine the full-scale output and percentage resolution

Ten-mark Questions

UNDERSTAND
1. Explain a binary ladder network of DAC with suitable diagram and expressions. List its advantages.
2. Explain the working of a 3-bit flash type ADC. List its advantages.
3. Explain the working of a successive approximation type ADC and compare its features with flash type ADC.
4. Explain the working of a dual-slope type ADC and summarize its advantages.

APPLICATION
1. Show how dual-slope ADC can be used to convert analog signal into digital form with circuit and relevant waveforms.
2. (a) Calculate the resolution of a 4 bit DAC in terms of percentage of full-scale voltage
   (b) For a 5-bit resistive divider, determine the following i) The weight assigned to the LSB.
   ii) The change in the output voltage due to a change in the LSB. iii) The output voltage for a digital input of 10110. Assume logical 0= 0 V and 1= + 10 V.

<div align="center">

Unit 5: Memories and programmable devices

Five-mark Questions

</div>

REMEMBER
1. Describe the role of memories in computers
2. List the memory types based on fabrication material and data retention
3. List the features of DDR memory
4. List the features of flash memory
5. List the features of magnetic memories
6. List he features of PLA

UNDERSTAND
1. Classify the memories based on speed and fabrication material
2. Distinguish between (i) ROM and RAM memories and (ii) Flash and Magnetic memories
3. Compare the features of static and dynamic RAM
4. Explain the working principle of Dynamic RAM cell
5. Relate the memory capacity and address range with examples
6. Compare PLA and PAL

APPLICATION
1. Calculate the address lines required to access 512 Kilo bytes of memory and calculate how many bytes of memory can be accessed with 15 address lines assuming byte addressable memory
2. Identify the functional pins required for RAM IC
3. Show how PAL can be used to implement simple Boolean expressions

<div align="center">

Ten-mark Questions

</div>

UNDERSTAND
1. (a) Compare volatile and non-volatile memories
   (b) Compare PLA and PAL
2. (a) Explain the working principle of static RAM cell
   (b) Compare the features of DDR1 and DDR2 memories

APPLICATION
1. Show how the PAL–type array should be programmed in order to implement each of the following SOP expressions. Use a mark **X** to indicate an intact fuse. Simplify the expressions, if necessary.   a) $Y = A\bar{B}C + \bar{A}B\bar{C} + ABC$ b) $Y = A\bar{B}C + \bar{A}BC + AB\bar{C} + \bar{A}BC$
2. A certain memory is specified as 32k x8.Determine a) the number of bits in each word b) the number of words being stored c) the number of memory cells d) the number of address input lines, e) the number of data input lines and f) the number of data output lines.
3. The 2125A is a static RAM IC that has a capacity of 1Kx1, one active-LOW chip select input, and separate data input and output. Show how to combine several 2125A ICs to form a 1Kx8 module.
4. Two 16 MB RAMS are used to build a RAM capacity of 32 MB. Show the configuration and also state the address inputs for which the two RAMs will be active. The two RAMs have common I/O pins, a write enable input that is active-LOW, and a chip select input that is active –HIGH.
5. (a) List the features and applications of E^2PROM.
   (b) List types and features of disk memories.
6. (a) Explain accessing process in (i) Magnetic memories and (ii) RAM

(b) List the features of DDR memory

Unit 6: Digital integrated circuits
Five-mark Questions

REMEMBER
1. Define fan-in, fan-out, propagation delay, power dissipation and noise margin as applicable to logic families
2. Describe briefly the operation of TTL NAND gate with circuit
3. List the features of ECL family
4. List the features of CMOS family

UNDERSTAND
1. Compare CMOS family with TTL family
2. Distinguish between HMOS and CHMOS
3. Explain the functioning of CMOS inverter
4. Classify the Integrated circuits based on the scale of integration.

APPLICATION
1. List the advantages and disadvantages of CMOS
2. List the voltage levels of TTL family

Ten-mark Questions

APPLICATION
1. a) Show how a CMOS buffer can drive a TTL load.
   b) List the advantages of CMOS devices.
2. a) Illustrate interfacing of TTL gate/circuit to CMOS gate/circuit.
   b) Explain the interfacing of CMOS devices to TTL devices.

End